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AMENDMENT

Please amend the application as indicated hereafter.

In the Claims:

Claim 1 (currently amended) A method of IP characterization, comprising:

providing an IP component;

automatically generating a plurality of test patterns for all paths in the IP component;

sequentially inputting the test patterns into the IP component for simulation, and outputting a plurality of corresponding simulation results; ~~and~~

~~generating an IP characteristic library based on the simulation results~~

extracting at least one key data from each of the simulation results, respectively; and

integrating the key data of each of the simulation results to generate the IP characteristic library.

Claim 2 (original) The method of IP characterization of claim 1, wherein the step of automatically generating the plurality of test patterns for all paths in the IP component comprises:

automatically searching all of the paths in the IP component; and

generating the corresponding test patterns for each of the paths.

Claim 3 (original) The method of IP characterization of claim 2, wherein the step of automatically searching all of the paths in the IP component comprises:

identifying and excluding an ESD path;

wherein if there is at least a path point which has not been completely searched, the path point is selected;

determining whether one of the paths of the selected path point reaches an end point

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of the path or not;

searching a next path point connected by one of the paths of the selected path point

by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point

by selecting a connection terminal of a resistor based on a resistor rule.

Claim 4 (original) The method of IP characterization of claim 3, wherein the step of

automatically searching all of the paths in the IP component further comprises:

analyzing a type of all of the I/O ports in the IP component; and

comparing the I/O ports of the IP component with an I/O port information stored in a

database.

Claim 5 (original) The method of IP characterization of claim 4, wherein the type of

the I/O ports comprises an input port, an output port and a bi-directional port.

Claim 6 (original) The method for IP characterization of claim 3, wherein the step of

automatically searching all of the paths in the IP component further comprises excluding

any path which is input/output from any of the I/O ports in the IP component not passing

through any circuitry in the IP component.

Claim 7 (canceled)

Claim 8 (original) The method of IP characterization of claim 1, wherein the IP

characteristic library comprises a plurality of timing information and a plurality of power

information corresponding to the test patterns.

Claim 9 (original) The method for IP characterization of claim 1, wherein the IP

component is configured by a Hardware Description Language (HDL).

Claim 10 (currently-amended) A method of finding paths in an IP component,

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comprising: providing an IP component;

identifying and excluding an ESD path; wherein if there is at least a path point which has not been completely searched yet, the path point is selected;

determining whether or not one of the paths of the selected path point reaches an end point of the path;

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a resistor based on a resistor rule.

Claim 11 (currently amended) The method of finding paths in an IP component of claim 10, further comprising: analyzing a type of all of the I/O ports in the IP component; and comparing the I/O ports of the IP component with an I/O port information stored in a database.

Claim 12 (currently amended) The method of finding paths in an IP component of claim 11, wherein a type of the I/O ports comprises an input port, an output port and a bi-directional port.

Claim 13 (currently amended) The method of finding paths in an IP component of claim 10, further comprising excluding any path which is input/output from any of the I/O ports in the IP component not passing through any circuitry in the IP component.

Claim 14 (currently amended) The method of finding paths in an IP component of claim 10, wherein the IP component is configured by a Hardware Description Language (HDL).

Claim 15 (currently amended) A computer readable recording media medium for

storing a ~~computer readable~~ program ~~implemented by~~ executing an IP characterization method on a computer system, ~~the program comprising a plurality of following instructions~~ the IP characterization method comprises:

reading an IP component;

automatically generating a plurality of test patterns for all paths in the IP component;

sequentially reading each of the test patterns for performing simulation on the IP component and generating a plurality of corresponding simulation results; ~~and~~

~~generating an IP characteristic library based on the simulation results~~

extracting at least one key data from each of the simulation results, respectively; and

integrating the key data of each of the simulation results to generate the IP characteristic library.

Claim 16 (currently amended) The computer readable recording ~~media~~ medium of claim 15, wherein ~~the instruction of~~ automatically generating the plurality of test patterns for all paths in the IP component comprises ~~a plurality of following instructions~~:

automatically searching all of the paths in the IP component; and

generating the corresponding test patterns for each of the paths.

Claim 17 (currently amended) The computer readable recording ~~media~~ medium of claim 16, wherein ~~the instruction of~~ automatically searching all of the paths in the IP component comprises:

identifying and excluding an ESD path;

wherein if there is at least a path point which has not been completely searched, the path point is selected;

determining whether or not one of the paths of the selected path point reaches an end

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point of the path;

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a resistor based on a resistor rule.

Claim 18 (currently amended) The computer readable recording ~~media~~ medium of claim 17, wherein ~~the instruction of~~ automatically searching all of the paths in the IP component further comprises:

analyzing a type of all of the I/O ports in the IP component; and

comparing the I/O ports of the IP component with an I/O port information stored in a database.

Claim 19 (currently amended) The computer readable recording ~~media~~ medium of claim 18, wherein a type of the I/O ports comprises an input port, an output port and a bi-directional port.

Claim 20 (currently amended) The computer readable recording ~~media~~ medium of claim 17, wherein ~~the instruction of~~ automatically searching all of the paths in the IP component further comprises excluding any path which is input/output from any of the I/O ports in the IP component and not passed through any circuitry in the IP component.

Claim 21 (canceled)

Claim 22 (currently amended) The computer readable recording ~~media~~ medium of claim 15, wherein the IP characteristic library comprises a plurality of timing information and a plurality of power information corresponding to the test patterns.

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Claim 23 (currently amended) The computer readable recording ~~media~~ medium of

claim 15, wherein the IP component is configured by a Hardware Description Language

(HDL).

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